SONA COLLEGE OF TECHNOLOGY, SALEM-5

(An Autonomous Institution)

M.E- Electronics and Communication Engineering

(VLSI Design)

CURRICULUM and SYLLABI

[For students admitted in 2018-2019]

M.E / M.Tech Regulation 2015

Approved by BOS and Academic Council meetings

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME I Semester under Regulations 2015
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit
Theory						
1	P15VLD101	Applied Mathematics for Electronics Engineers	3	2	0	4
2	P15VLD102	DSP Integrated Circuits	3	0	0	3
3	P15VLD103	Advanced Digital System Design	4	0	0	4
4	P15VLD104	CMOS VLSI Design	3	0	0	3
5	P15VLD105	Solid State Device Modeling and Simulation	3	0	0	3
6	P15VLD106	Testing of VLSI Circuits	3	0	0	3
Practical						
7	P15VLD107	VLSI Design Laboratory - I	0	0	4	2
					Total Credits	**22**

Approved by

Chairman, Electronics and Communication Engineering BOS
Dr.R.S.Sabeenian

Member Secretary, Academic Council
Dr.R.Shivakumar

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

Copy to:-
HOD/ECE, First Semester ME VLSI Students and Staff, COE

Sona College of Technology, Salem
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Courses of Study for ME II Semester under Regulations 2015
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit
Theory						
1	P15VLD201	VLSI Signal Processing	3	2	0	4
2	P15VLD202	Computer Aided Design of VLSI Circuits	4	0	0	4
3	P15VLD203	Low Power VLSI Design	3	0	0	3
4	P15VLD501	**Professional Elective -** Analysis and Design of Analog Integrated Circuits	3	0	0	3
5	P15VLD512	**Professional Elective -** Embedded Systems	3	0	0	3
6	P15VLD513	**Professional Elective -** Nanoelectronics	3	0	0	3
Practical						
7	P15VLD204	VLSI Design Laboratory - II	0	0	4	2
					Total Credits	**22**

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Sona College of Technology, Salem
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Courses of Study for ME III Semester under Regulations 2015
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit
Theory						
1	P15VLD509	**Professional Elective**- ASIC Design	3	0	0	3
2	P15VLD511	**Professional Elective**- Analysis and Design of Digital Integrated Circuits	3	0	0	3
3	P15VLD607	**Open Elective**- Human Resource Development	3	0	0	3
Practical						
4	P15VLD301	Project Phase - I	0	0	16	8
					Total Credits	**17**

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Sona College of Technology, Salem
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Courses of Study for ME IV Semester under Regulations 2015
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit
Practical						
1	P15VLD401	Project Phase – II	0	0	24	12
					Total Credits	**12**

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Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME I Semester under Regulations 2015
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit
Theory						
1	P15VLD101	Applied Mathematics for Electronics Engineers	3	2	0	4
2	P15VLD102	DSP Integrated Circuits	3	0	0	3
3	P15VLD103	Advanced Digital System Design	4	0	0	4
4	P15VLD104	CMOS VLSI Design	3	0	0	3
5	P15VLD105	Solid State Device Modeling and Simulation	3	0	0	3
6	P15VLD106	Testing of VLSI Circuits	3	0	0	3
Practical						
7	P15VLD107	VLSI Design Laboratory - I	0	0	4	2
					Total Credits	**22**

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HOD/ECE, First Semester ME VLSI Students and Staff, COE

P15VLD101	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	L	T	P	C	Marks
		3	2	0	4	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Comprehend main concepts and propositions of fuzzy logic principles.
2. Apply the various methods of matrix factors to solve the engineering problems.
3. Use the decompositions of the matrix and rank reducing approximations for engineering applications.
4. Apply and analyze the dynamic programming for problem solving.
5. Analyze problem solving capability of queuing models.

UNIT I	**FUZZY LOGIC** Classical Logic – Multi Valued Logics – Basic Concepts of Fuzzy Sets – Fuzzy Complements – Fuzzy Propositions – Equivalence and Similarity Relations – Problems on Fuzzy Propositions – Fuzzy Quantifiers.	**15**
UNIT II	**MATRIX THEORY** Some Important Matrix Factorizations –The Cholesky's Factorization – Unitary Matrices – Least Square Filters – Computing the QR Factorization – House Holder Transformations – QR Factorization Using Given Rotations.	**15**
UNIT III	**SINGULAR VALUE DECOMPOSITION** Pseudo Inverses and the SVD – Rank Reducing Approximations – Effective Rank – Application of SVD – Toplitz Matrices and Some Applications – Durbin's Algorithm – Optimal Predictors and Toplitz Inverses – Toplitz Equations with a General RHS.	**15**
UNIT IV	**DYNAMIC PROGRAMMING** Recursive Nature of Computations in DP – Forward and Backward Recursion – Selected DP Applications – Knapsack Loading Model – Work Force Size Model – Equipment Replacement Model – Inventory Models – Problem of Dimensionality.	**15**
UNIT V	**QUEUING MODELS** Poisson Process – Markovian Queues – Single and Multi-Server Models (Problems Only) – Little's Formula – Steady State Analysis – Self Service Queue.	**15**
		Total: 75

REFERENCE BOOKS

1.	George J. Klir and Yuan, B., "*Fuzzy Sets and Fuzzy Logic, Theory and Applications"*, Prentice – Hall of India Pvt. Ltd., 1997.
2.	Moon, T.K., Sterling, W.C., "*Mathematical Methods and Algorithms for Signal Processing"*, Pearson Education, 2000.
3.	Richard Johnson, Miller & Freund's, "*Probability and Statistics for Engineers"*, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi, 2007.
4.	Taha, H.A., "*Operations Research, An introduction"*, 7th Edition, Pearson Education Editions, Asia, New Delhi, 2002.
5.	Donald Gross and Carl M. Harris, "*Fundamentals of Queuing theory"*, 2nd Edition, John Wiley and Sons, New York, 1985.

P15VLD102	DSP INTEGRATED CIRCUITS	L	T	P	C	Marks
		3	0	0	3	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Design and apply standard DSP and other DSP systems used in ICs.
2. Design and illustrate the concepts of DSP systems, DFT, FFT and DCT.
3. Design the digital filters IIR and FIR for signal processing applications.
4. Examine and synthesize the DSP architectures and implement it on PEs and bit serial PEs.
5. Design and evaluate recent trends in DSP processors and system design.

UNIT I	**DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES** Standard Digital Signal Processors – Application Specific IC's for DSP – DSP System – Facets – DSP System Design – Partitioning Techniques – Integrated Circuit Design – MOS transistors – MOS logic – VLSI process Technologies – Trends in CMOS Technologies.	**9**
UNIT II	**DIGITAL SIGNAL PROCESSING** Digital Signal Processing – Sampling of Analog Signals – Selection of Sample Frequency – Signal-Processing Systems – Frequency Response – Transfer Functions – Signal Flow Graphs – Filter Structures – Adaptive DSP Algorithms – DFT – The Discrete Fourier Transform – FFT – The Fast Fourier Transform Algorithm – Image Coding – Discrete Cosine Transforms.	**9**
UNIT III	**DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS** FIR Filters – FIR Filter Structures – FIR Chips- IIR filters – Specifications of IIR Filters – Mapping of Analog Transfer Functions – Mapping of Analog Filter Structures – Multi-rate Systems – Interpolation with an Integer Factor – Sampling Rate Change with a Ratio L/M – Multi-rate Filters – Finite Word Length Effects –Parasitic Oscillations – Scaling of Signal Levels – Round-Off Noise – Measuring Round-Off Noise – Coefficient Sensitivity –Sensitivity and Noise	**9**
UNIT IV	**DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES** Introduction – DSP System Architectures – Standard DSP Architecture – Ideal DSP Architectures – Multiprocessors and Multi-Computers – Systolic and Wave Front Arrays – Shared Memory Architectures – Mapping of DSP Algorithms onto Hardware – Implementation Based on Complex PEs – Shared Memory Architecture With Bit – Serial PEs.	**9**
UNIT V	**DSP PROCESSOR AND RECENT TRENDS IN DSP SYSTEM DESIGN** Introduction of TMS320C55X Processors – Features – CPU Architecture of C55X – Memory Architecture – Addressing Modes – Assembly Language Instructions – Pipeline Operation – Interrupts – Peripherals – An Overview of the Application Notes on DSP Systems – An Overview of Open Multimedia Application (OMAP) – Evolution of FPGA Based System Design – An Introduction to FPGA – Design flow for an FPGA Based System Design – CAD Tools for FPGA Based System Design – Soft-Core Processor – FPGA based DSP System Design.	**9**
		Total: 45

REFERENCE BOOKS

1. Lars Wanhammer, "*DSP Integrated Circuits"*, Academic press, New York, 1999.
2. Venkataramani B. and Bhaskar M., "*Digital Signal Processors – Architecture, Programming and Applications"*, Tata McGraw – Hill Publishing Company Limited, New Delhi, 2011.
3. Emmanuel C. I. Feachor, Barrie W. Jervis, "*Digital signal processing – A Practical Approach"*, 2nd Edition, Pearson Education, Asia 2001.
4. Bayoumi & Magdy A., "*VLSI Design Methodologies for Digital Signal Processing Architectures"*, BS Publications, 2005.

P15VLD103	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C	Marks
		4	0	0	4	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Design and analyze the synchronous sequential circuits.
2. Design and analyze synchronous sequential circuits using ASM.
3. Design and analyze asynchronous sequential circuits.
4. Analyze and verify variable entered maps.
5. Design system controllers using combinational and sequential circuits.

UNIT I	**SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN** Structure and Operation of Clocked Synchronous Sequential Networks – Analysis of Clocked Synchronous Sequential Circuits – Modeling of Clocked Synchronous Sequential Network Behavior – Serial Binary Adder Using Mealy and Moore Networks – Sequence Recognizer – State Table Reduction – State Assignment – Design of Clocked Synchronous Sequential Circuits.	**12**
UNIT II	**SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN USING ASM** Algorithmic State Machine – ASM Charts – ASM Blocks – Sequence Recognition Using ASM Charts – State Assignments – ASM Transition Tables – ASM Excitation Tables – ASM Realization Using Discrete Gates – Multiplexers – PLAs – PROMs – Design of Iterative Circuits.	**12**
UNIT III	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN** Structure and Operation of Asynchronous Sequential Networks – Analysis of Asynchronous Sequential Circuit – Races and Hazards in Asynchronous Sequential Networks – Primitive Flow Table – Reduction of Input Restricted Flow Tables – Flow Table Reduction – State Assignment Problem and the Transition Table - Design of Asynchronous Sequential Circuits.	**12**
UNIT IV	**VEM AND MULTI-INPUT SYSTEM CONTROLLER DESIGN** Variable Entered Maps – Simplification – System Controllers – Design Phases – MDS Diagram Generation – MDSD Symbology – Choosing The Controller Architecture – State Assignment – Next State Decoder – Examples of 2's Complement System and Pop Vending Machine – Concepts Related to the Use of Conditional Outputs.	**12**
UNIT V	**SYSTEM CONTROLLERS USING COMBINATIONAL AND SEQUENTIAL CIRCUITS** Decoders and Multiplexers in System Controllers – Indirect-Addressed MUX Configuration – System Controllers Using Shift Registers and Counters – General Requirements of a Programmable Controller – Microinstructions – Programmable Controllers with Fixed Instruction Set.	**12**
		Total: 60

REFERENCE BOOKS

1. Donald G. Givone, "*Digital principles and Design"*, Tata McGraw Hill, 2013.
2. William I. Fletcher, "*An Engineering Approach to Digital Design"*, Prentice Hall India, 2009.
3. Charles H. Roth Jr,, "*Fundamentals of Logic design"*, Thomson Learning, 2004.
4. Nripendra N Biswas, "*Logic Design Theory"*, Prentice Hall of India, 2005.

P15VLD104	CMOS VLSI DESIGN	L	T	P	C	Marks
		3	0	0	3	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Illustrate the VLSI design and fabrication processes of MOSFETs.
2. Describe and evaluate the MOSFET operations and modeling of MOSFETS.
3. Analyze and evaluate the static and switching characteristics of CMOS inverters.
4. Design combinational and sequential logic circuits using CMOS principles.
5. Write the programming codes, simulate and implement CMOS logic circuits using Verilog HDL.

UNIT I	**INTRODUCTION AND FABRICATION OF MOSFETS** Overview of VLSI Design Methodologies – VLSI Design Flow – Design Hierarchy – Concepts of Regularity, Modularity and Locality – VLSI Design Styles – Design Quality – Packaging Technology – Fabrication Process Flow Basic Steps – The CMOS n-Well Process – Layout Design Rules – Full-Custom Mask Layout Design.	**9**
UNIT II	**MOS TRANSISTORS AND IT'S MODELING USING SPICE** The MOS Structure – The MOS System under External Bias – Structure and Operation of MOS Transistor – MOSFET Current-Voltage Characteristics – MOSFET Scaling and Small-Geometry Effects – MOSFET Capacitances – Basic Concepts of Modeling of MOS – The LEVEL 1 Model Equations – The LEVEL 2 Model Equations – The LEVEL 3 Model Equations – State-of-the-Art MOSFET Models – Capacitance Models – Comparison of the SPICE MOSFET Models.	**9**
UNIT III	**MOS INVERTERS AND CHARACTERISTICS** Static Characteristics of Resistive Load Inverter – Inverters with n-Type MOSFET Load – CMOS Inverter – Introduction of Switching Characteristics – Delay Time – Determination of delay Times – Inverter Design with Delay Constraints – Estimation of Interconnect Parasitics – Calculation of Interconnect Delay – Switching power Dissipation of CMOS inverters.	**9**
UNIT IV	**COMBINATIONAL AND SEQUENTIAL CMOS LOGIC CIRCUITS** MOS Logic Circuits with Depletion nMOS Loads – CMOS Logic Circuits – CMOS Complex Logic Circuits – CMOS Transmission Gates – Behavior of Bistable Elements – CMOS SR Latch Circuit – CMOS Clocked Latch and CMOS Flip – Flop Circuits – CMOS D-Latch and CMOS Edge-Triggered Flip-Flop.	**9**
UNIT V	**VERILOG HARDWARE DESCRIPTION LANGUAGE** Overview of Digital Design with Verilog HDL – Hierarchical Modeling Concepts – Modules and Ports – Gate Level Modeling – Data Flow Modeling – Behavioral Modeling – Task & Functions – Design and Implementation of Test Bench.	**9**
		Total: 45

REFERENCE BOOKS

1. Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits - Analysis and Design",* McGraw Hill Education (India) Pvt. Ltd., 3rd Edition, 2003
2. Bhaskar J., "*A Verilog HDL Primer",* B. S. Publications, 2nd Edition, 2001.
3. R. Jacob Baker, "*CMOS circuit design, Layout, and Simulation"*, John Wiley and Sons, 2012.
4. Neil H.E. Weste and Kamran Eshraghian, "*Principles of CMOS VLSI Design - A System Perspective",* Pearson Education ASIA, 2nd Edition, 2000.
5. John P. Uyemura, "*Introduction to VLSI Circuits and Systems",* John Wiley & Sons, Inc., 2002.

P15VLD105	SOLID STATE DEVICE MODELING AND SIMULATION	L	T	P	C	Marks
		3	0	0	3	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Comprehend and analyze MOSFET device operation and RF modeling.
2. Analyze and illustrate the modeling technique for noise and its distortion.
3. Design and analyze the modeling of BSIM4 MOSFET models.
4. Design and evaluate the EKV model and other MOSFET models.
5. Analyze the modeling of passive devices and quality assurance of MOSFET models.

UNIT I	**MOSFET DEVICE PHYSICS, OPERATION AND RF MODELING** The MOS Capacitor – Threshold Voltage – MOS Capacitance – MOS Charge Control Model – Basic MOSFET Operation – Basic MOSFET Modeling – Advanced MOSFET – Equivalent Circuit Representation of MOS Transistors – High-frequency Behavior of MOS Transistors and AC Small-Signal Modeling – Model Parameter Extraction – NQS Model for RF Applications.	**9**
UNIT II	**NOISE MODELING AND DISTORTION ANALYSIS** Noise Sources in a MOSFET – Flicker Noise Modeling – The Physical Mechanisms of Flicker Noise – Flicker Noise Models – Thermal Noise Modeling – Existing Thermal Noise Models – HF Noise Parameters – Analytical Calculation of the Noise Parameters – Basic Terminology – Non-linearities in CMOS Devices and Their Modeling – Calculation of Distortion in Analog CMOS Circuits.	**9**
UNIT III	**BSIM4 MOSFET MODEL** An Introduction to BSIM4 – Gate Dielectric Model –Threshold Voltage Model – Channel Charge Model – Mobility Model – Source/Drain Resistance Model – *I-V* Model – Gate Tunneling Current Model – Substrate Current Models – Capacitance Models – High-Speed (Non-Quasi-Static) Model –RF Model – Noise Model.	**9**
UNIT IV	**OTHER MOSFET MODELS** Introduction - Model Features – Long-Channel Drain Current Model – Modeling Second-Order Effects of the Drain Current – SPICE Example – The Effect of Charge-Sharing – Modeling of Charge Storage Effects – Non-Quasi-Static Modeling – The Noise Model – Temperature Effects – MOS Model 9 – The MOSA1 Model.	**9**
UNIT V	**MODELING OF PASSIVE DEVICES, PROCESS VARIATION AND QUALITY ASSURANCE OF MOSFET MODELS** Introduction – Resistors – Well Resistor – Metal Resistor – Diffused Resistor – Poly Resistor – Capacitors – Poly-Poly Capacitors – Metal-Insulator-Metal Capacitors – MOSFET Capacitors – Junction Capacitors – Inductors – The Influence of Process Variation and Device Mismatch – Modeling of Device Mismatch for Analog/RF Applications – Motivation – Benchmark Circuits and Automation of the Tests.	**9**
		Total: 45

REFERENCE BOOKS

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, "*Device Modeling for Analog and RF CMOS Circuit Design"*, John Wiley & Sons Ltd, 2003.
2. Grasser, T., "*Advanced Device Modeling and Simulation"*, World Scientific Publishing Company, 2003.
3. Ben G. Streetman, "*Solid State Devices"*, Prentice Hall, 1997.
4. Carlos Galup-Montoro, Marco Cherem Schneider, "*MOSFET Modeling for Circuit Analysis and Design"*, World Scientific Publishing Co. Pte. Ltd., 2007.

P15VLD106	TESTING OF VLSI CIRCUITS	L	T	P	C	Marks
		3	0	0	3	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Analyze the modeling of faults and types of simulation for testing circuits and systems.
2. Design and analyze test generation of combinational circuits and testable designs.
3. Design and analyze test generation of sequential circuits and testable designs.
4. Design and evaluate the test pattern generation of Built In Self Test.
5. Synthesize and analyze different fault diagnosis in combinational and sequential circuits.

UNIT I	**TESTING AND FAULT MODELLING** Introduction to Testing – Faults in Digital Circuits – Modeling of Faults – Logical Fault Models – Fault Detection and Redundancy – Fault Equivalence and Fault Location – Fault Dominance – Logic Simulation – Types of Simulation – Compiled Simulation – Event Driven Simulation – Delay Models – Gate Level Event-Driven Simulation.	**9**
UNIT II	**TEST GENERATION OF COMBINATIONAL CIRCUITS** Test Generation of Combinational Logic Circuits – One Dimensional Path Sensitization – Boolean Difference – D-Algorithm – Path Oriented Decision Making – Detection of Multiple Faults in Combinational Logic Circuits – Testable Combinational Logic Circuit Design –The Reed-Muller Expansion Techniques – Three Level OR-AND - OR Design – Use of Control Logic – Syndrome Testable Design.	**9**
UNIT III	**TEST GENERATION OF SEQUENTIAL CIRCUITS** Test Generation of Sequential Circuits – Testing of Sequential Circuits as Iterative Combinational Circuits – State Table Verification – Random Testing – Transition Count Testing – Signature Analysis – Design of Testable Sequential Circuits – Scan Path Technique – Level Sensitive Scan Design – Random Access Scan Technique.	**9**
UNIT IV	**BUILT IN SELF – TEST** Introduction – Test Pattern Generation for BIST – Exhaustive Testing – Pseudorandom Testing – Pseudo-Exhaustive Testing – Specific BIST Architectures – Built In Evaluation and Self Test – Random Test Socket – LSSD on Chip Self Test – Self-Testing Using MISR and Parallel SRSG – Concurrent BIST Architecture – Random Test Data – Circular Self Test Path – Built In Logic Block Observation.	**9**
UNIT V	**FAULT DIAGNOSIS** Logic Level Diagnosis – Fault Dictionary- Guided Probe Testing – Diagnosis by UUT Reduction – Fault Diagnosis for Combinational Circuits – Expert Systems for Diagnosis – Effect Cause Analysis – Self Checking Design – Application of Error Detecting and Error Correcting Codes – Multiple Bit Errors – Checking Circuits and Self Checking – Self Checking Checkers – Parity Check Function – Totally Self Checking Checkers.	**9**
		Total: 45

REFERENCE BOOKS

1. Parag K. Lala, "*Fault Tolerant and Fault Testable Hardware Design"*, BS Publications, 2009.
2. Abramovici M, Breuer M.A. and Friedman A.D., "*Digital Systems and Testable Design"*, Jaico Publishing House, 2004.
3. Bushnell M.L and Agrawal V. D., "*Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuit"*, Kluwar Academic Publishers, 2002.
4. Crouch A.L, " *Design for Test for Digital IC's and Embedded Core System"*, Prentice Hall International, 2002.

P15VLD107	VLSI DESIGN LABORATORY – I	L	T	P	C	Marks
		0	0	4	2	100

COURSE OUTCOMES

At the end of the experiments, the students will be able to -

1. Design and analysis the digital systems using Verilog HDL.
2. Verify the characteristics of MOSFET.
3. Implement the digital system design in FPGA Board and analyze the same for performance.
4. Design the NMOS, CMOS Logic circuits and analyze the characteristics of the same.

LIST OF EXPERIMENTS

1. Design of NMOS and CMOS Inverters - DC and transient characteristics and switching times.
2. Design of CMOS logic gate circuits.
   i) Static logic
   ii)Dynamic logic
   iii) Domino logic
3. Design of combinational circuits using Verilog and implement in FPGA.
   i) Multiplexer and De-Multiplexer
   ii)Encoder and Decoder
   iii) Comparator
4. Design of sequential circuits using Verilog and implement in FPGA.
   i) Shift Registers
   ii)Counters
5. Design and implementation of ALU using FPGA and Verilog HDL.
6. Design of FIR filters using FPGA and Verilog HDL.
7. Design of the multiplier using FSM.
8. Model a sequence detector to checks three consecutive one's and verify the same using test bench.
9. Design and implementation of traffic controller using FPGA.

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Theory						
1	P15VLD201	VLSI Signal Processing	3	2	0	4
2	P15VLD202	Computer Aided Design of VLSI Circuits	4	0	0	4
3	P15VLD203	Low Power VLSI Design	3	0	0	3
4	P15VLD501	**Professional Elective -** Analysis and Design of Analog Integrated Circuits	3	0	0	3
5	P15VLD512	**Professional Elective -** Embedded Systems	3	0	0	3
6	P15VLD513	**Professional Elective -** Nanoelectronics	3	0	0	3
Practical						
7	P15VLD204	VLSI Design Laboratory - II	0	0	4	2
					Total Credits	**22**

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HOD/ECE, Second Semester ME VLSI Students and Staff, COE

P15VLD201	VLSI SIGNAL PROCESSING	L	T	P	C	Marks
		3	2	0	4	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

6. Discuss about the introduction of DSP systems, pipelining and parallel processing.
7. Analyze the different techniques of retiming, folding and unfolding
8. Explain the different algorithms used for fast convolution, pipelining, parallel and processing of IIR filters
9. Design the different types of multipliers and CSD Representation of VLSI systems.
10. Discuss about the synchronous and asynchronous pipelining and need for low power VLSI.

UNIT I	**INTRODUCTION TO DSP SYSTEMS** Introduction to DSP Systems – Typical DSP Algorithms – Iteration Bound – Data Flow Graph Representations – Loop Bound and Iteration Bound – Algorithms for Computing Iteration Bound – Pipelining and Parallel Processing – Pipelining of FIR Digital Filters – Parallel Processing – Pipelining and Parallel Processing for Low Power.	**15**
UNIT II	**RETIMING, FOLDING AND UNFOLDING** Retiming – Definitions and Properties – Retiming Techniques – Unfolding – an Algorithm for Unfolding – Properties of Unfolding –Applications – Sampling Period Reduction – Parallel Processing –Folding – Folding Transformation – Register Minimizing Techniques – Register Minimization in Folded Architectures.	**15**
UNIT III	**FAST CONVOLUTION** Fast Convolution – Cook-Toom Algorithm – Winograd Algorithm – Iterated Convolution – Cyclic Convolution – Pipelined and Parallel Recursive and Adaptive Filters – Pipeline Interleaving in Digital Filters – Pipelining in First – Order IIR Filters – Parallel Processing for IIR Filters – Combined Pipelining and Parallel Processing for IIR Filters – Pipelined Adaptive Digital Filters – Relaxed Look-Ahead – Pipelined LMS Adaptive Filter.	**15**
UNIT IV	**BIT-LEVEL ARITHMETIC ARCHITECTURES** Bit-Level Arithmetic Architectures – Parallel Multipliers – Baugh-Wooley Multipliers – Interleaved Floor – Plan and Bit-Plane – Based Digital Filters – Design of Lyon's Bit-Serial Multipliers using Horner's Rule – Bit-Serial FIR Filter –CSD Representation – CSD Multiplication using Horner's Rule for Precision Improvement – Distributed Arithmetic.	**15**
UNIT V	**PROGRAMMING DIGITAL SIGNAL PROCESSORS** Synchronous – Wave and Asynchronous Pipelining – Synchronous Pipelining and Clocking Styles – Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs –Wave Pipelining – Asynchronous Pipelining – Programming Digital Signal Processors – General Architecture with Important Features.	**15**
		Total: 75

REFERENCE BOOKS

3. Keshab K. Parhi, "*VLSI Digital Signal Processing systems, Design and implementation",* Wiley, Inter Science, 1999.
4. Mohammed Isamail and Terri Fiez*, "Analog VLSI Signal and Information Processing"*, Mc Graw-Hill, 1994.

P15VLD202	COMPUTER AIDED DESIGN OF VLSI CIRCUITS	L	T	P	C	Marks
		4	0	0	4	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Comprehend and analyze the VLSI design methodologies and algorithmic graph theory.
2. Analyze and illustrate layout design rules, placement and partitioning.
3. Design and analyze floor planning and routing concept.
4. Examine and verify the various modeling of simulation.
5. Analyze and illustrate synthesis and scheduling.

UNIT I	**VLSI DESIGN METHODOLOGIES AND ALGORITHMIC GRAPHY THEORY** Introduction to VLSI Design Methodologies – VLSI Design Automation Tools – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization	**12**
UNIT II	**PLACEMENT AND PARTITIONING** Layout Compaction – Design Rules - Problem Formulation – Algorithms for Constraint Graph Compaction – Placement And Partitioning – Circuit Representation – Wire length Estimation – Placement Algorithms – Partitioning.	**12**
UNIT III	**FLOORPLANNING AND ROUTING** Floor planning Concepts – Shape Functions and Floor Plan Sizing – Types of Local Routing Problems – Area Routing – Channel Routing – Global Routing – Algorithms for Global Routing.	**12**
UNIT IV	**SIMULATION AND VERIFICATION** VLSI Simulation – Gate-Level Modeling And Simulation – Switch-Level Modeling and Simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis.	**12**
UNIT V	**HIGH LEVEL SYNTHESIS** Hardware Models for High Level Synthesis – Internal Representation of the Input Algorithm – Allocation-Assignment and Scheduling – Scheduling Algorithm – Assignment problem – High Level Transformations.	**12**
		Total: 60

REFERENCE BOOKS

1.	Gerez S.H., "*Algorithms for VLSI Design Automation"*, John Wiley & Sons, 2009.
2.	Sherwani N.A., "*Algorithms for VLSI Physical Design Automation*" Kluwar Academic Publishers, 2002
3.	Drechsler, R., "*Evolutionary Algorithms for VLSI CAD"*, Kluwer Academic Publishers, Boston, 1998.
4.	Hill, D., Shugard D., Fishburn J. and Keutzer K., "*Algorithms and Techniques for VLSI Layout Synthesis"*, Kluwer Academic Publishers, Boston, 1989.

P15VLD203	LOW POWER VLSI DESIGN	L	T	P	C	Marks
		3	0	0	3	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Discuss about the sources of power consumption in CMOS and hierarchy of limits
2. Calculate the power estimation in CMOS at logic level and circuit level.
3. Analyze the synthesis and software design for low power.
4. Describe the SOI CMOS Devices.
5. Know how to synthesis SOI CMOS digital and analog circuits.

UNIT I	**POWER DISSIPATION IN CMOS** Introduction – Sources of Power Dissipation – Designing for Low power – Physics of Power Dissipation in MOSFET Devices – Power Dissipation in CMOS – Hierarchy of Limits of Power – Fundamental-Material-Device-Circuit and System limits.	**9**
UNIT II	**POWER ESTIMATION** Modeling of Signals – Signal Probability Calculation – Probabilistic Techniques for Signal Activity Estimation – Statistical Techniques – Estimation of Glitching Power – Sensitivity Analysis – Power Estimation Using Input Vector Compaction – Power Dissipation in Domino CMOS – Circuit Reliability – Power Estimation at the Circuit Level – High Level Power Estimation – Information-Theory-Based Approaches – Estimation of Maximum power.	**9**
UNIT III	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER** Behavioral Level Transforms – Logic Level Optimization for Low power – Circuit Level – Sources of Software Power Dissipation – Software Power Estimation – Software Power Optimizations – Automated Low-Power Code Generation – Co-design for Low Power.	**9**
UNIT IV	**SOI CMOS DEVICE** Introduction – Basic SOI Technology – Back Gate Bias Effects – Short Channel Effects – Narrow Channel Effects – Mobility – Floating Body Effects – Subthreshold Behavior – Impact Ionization – Breakdown – Transient-Induced Leakage – Self-Heating – Hot Carriers – Accumulation-Mode Devices.	**9**
UNIT V	**SOI CMOS DIGITAL AND ANALOG CIRCUITS** Static and Dynamic Logic Circuits – DRAM – SRAM – CAM – Gate Array – CPU – Multiplier and DSP – Frequency Divider – SOI Op Amps – Filters – ADC and DAC – Sigma – Delta ADC – RF Circuits Sigma – Low Noise Amplifier – Mixer – Voltage Controlled Oscillator.	**9**
		Total: 45

REFERENCE BOOKS

1. Roy K. and Prasad S.C. , "*Low Power CMOS VLSI circuit design,"* Wiley,2011.
2. James B. Kuo, Shin chia Lin, *"Low voltage SOI CMOS VLSI Devices and Circuits"*, John Wiley and sons, inc 2008.
3. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "*Designing CMOS Circuits For Low Power"*, Kluwer, 2002.
4. Kuo J.B and Lou J.H, "*Low voltage CMOS VLSI Circuits"*, Wiley 1999

P15VLD204	VLSI DESIGN LABORATORY – II	L	T	P	C	Marks
		0	0	4	2	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Design and simulate the performance analysis of source followers, and OP- AMPs.
2. Design and simulate different types of current mirrors.
3. Design and simulate the gate –level and switch – level modeling methods.
4. Implementation of Stepper Motor Control using FPGA.
5. Design and implement the elevator controller, alarm clock controller, model train controller

LIST OF EXPERIMENTS

1.	Design and simulate frequency response and noise analysis of any Source followers.
2.	Design and simulate operational amplifier performance parameters - One-stage Op Amps, Two-stage Op Amps.
3.	Design and implementation of BIT - SLICE using FPGA.
4.	Design and simulate cascode current mirrors and active current mirrors.
5.	Design and Simulation of Gate-level modeling.
6.	Design and Simulation of Switch-level modeling.
7.	Implementation of Stepper motor controller using FPGA.
8.	Implementation of Elevator controller using Embedded Microcontroller.
9.	Implementation of Alarm Clock controller using Embedded Microcontroller.
10.	Implementation of Model Train controller using Embedded Microcontroller.

P15VLD501	ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS	L	T	P	C	Marks
		3	0	0	3	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Design the single stage amplifiers using PMOS and NMOS driver circuits
2. Describe and analyze the concepts of single stage amplifiers and noise characteristics associated with amplifiers.
3. Illustrate and analyze the types of current mirrors, active loads and the concepts of voltage and current reference circuits.
4. Analyze the Op Amps circuits and frequency compensation of ICs.
5. Synthesize the stability and frequency compensation of Op-Amps.

UNIT I	**SINGLE STAGE AND DIFFERENTIAL AMPLIFIERS** Basic Concepts – Common Source Stage – Source Follower – Common Gate Stage – Cascode Stage – Single Ended and Differential Operation – Basic Differential Pair – Differential Pair With MOS Loads – Gilbert Cell.	**9**
UNIT II	**FREQUENCY RESPONSE AND NOISE ANALYSIS** Miller Effect – Association of Poles with Nodes – Frequency Response of Common Source Stage – Source Followers – Common Gate Stage – Cascode Stage – Differential Pair – Statistical Characteristics of Noise – Noise in Single Stage Amplifiers – Noise in Differential Amplifiers – Noise Bandwidth.	**9**
UNIT III	**CURRENT MIRRORS, ACTIVE LOADS AND REFERENCES** Current Mirrors – Simple Current Mirrors – Cascode Current Mirrors – Wilson Current Mirrors – Active Loads – Common Emitter/Common Source Amplifier with Complementary Load – Common Emitter/Common Source Amplifier with Depletion Load – Common Emitter/Common Source Amplifier with Diode-Connected Load – Differential Pair with Current-Mirror Load – Low-Current Biasing – Supply Insensitive Biasing – Temperature Insensitive Biasing.	**9**
UNIT IV	**OPERATIONAL AMPLIFIERS** Basic Concept of Op Amp – Deviations from Ideality in Real Operational Amplifiers – Basic Two Stage MOS Operational Amplifiers – Two Stage MOS Operational Amplifiers with Cascodes – MOS Telescopic-Cascode Operational Amplifiers – MOS Folded-Cascode Operational Amplifiers – MOS Active-Cascode Operational Amplifiers.	**9**
UNIT V	**STABILITY AND FREQUENCY COMPENSATION** General considerations – Multipole systems – Phase Margin – Frequency Compensation – Compensation of Two-Stage Op Amps – Slew Rate – Methods of Improving Slew – Rate in Two Stage Op Amps – Improving Slew Rate in MOS Op Amps.	**9**
		Total: 45

REFERENCE BOOKS

1.	Behzad Razavi, "*Design of Analog CMOS Integrated Circuits"*, Tata McGraw Hill, 2001.
2.	Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "*Analysis and Design of Analog Integrated Circuits"*, 5th Edition, Wiley, 2009.
3.	Grebene, "*Bipolar and MOS Analog Integrated circuit design"*, John Wiley & sons, Inc., 2003.

P15VLD512	EMBEDDED SYSTEMS	L	T	P	C	Marks
		3	0	0	3	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Illustrate the basic architecture of embedded system.
2. Analyze the ARM and SHARC processors.
3. Analyze and describe about the different networks in the embedded system
4. Compute the real time characteristics of embedded system
5. Design the techniques used to describe the embedded system design.

UNIT I	**EMBEDDED ARCHITECTURE** Embedded Computers – Characteristics of Embedded Computing Applications – Challenges in Embedded System Design – Embedded System Design Process – Requirements – Specification and Architectural Design – Designing Hardware and Software Components – System Integration.	**9**
UNIT II	**EMBEDDED PROCESSOR AND COMPUTING PLATFORM** ARM Processor – Processor and Memory Organization – Data Operations – Flow of Control – SHARC Processor Memory Organization – Data Operations – Flow of Control – Parallelism with instructions – CPU Bus Configuration – ARM Bus – SHARC Bus – Memory Devices – Input / Output Devices – Design Example: Alarm Clock..	**9**
UNIT III	**NETWORKS** Distributed Embedded Architecture – Hardware and Software Architectures – Networks for Embedded Systems – I^2C – CAN Bus – SHARC link ports – Ethernet – Myrinet – Internet – Design Example: Elevator Controller.	**9**
UNIT IV	**REAL-TIME CHARACTERISTICS** Clock Driven Approach – Weighted Round Robin Approach – Priority Driven Approach – Dynamic Versus Static Systems – Effective Release Times and Deadlines – Optimality of the Earliest Deadline First (EDF) Algorithm – Off-line Versus On-Line Scheduling.	**9**
UNIT V	**SYSTEM DESIGN TECHNIQUES** Design Methodologies – Requirement Analysis – Specification – System Analysis and Architecture Design – Quality Assurance – Design Example: Telephone PBX-Ink Jet Printer – Personal Digital Assistants – Set-Top Boxes.	**9**
		Total: 45

REFERENCE BOOKS

1. Wayne Wolf, *"Computers as Components: Principles of Embedded Computing System Design"*, Morgan Kaufman Publishers, 2001.
2. Jane. W.S. Liu, " *Real-Time systems"*, Pearson Education Asia, 2000
3. Frank Vahid and Tony Givargi, "*Embedded System Design: A Unified Hardware/Software Introduction"*, John Wiley & Sons, 2000
4. Krishna C. M and Shin K. G., "*Real-Time Systems"*, McGraw-Hill, 1997

P15VLD513	NANOELECTRONICS	L	T	P	C	Marks
		3	0	0	3	100

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Design and illustrate circuit design using FINFET.
2. Design SRAM, NRAM, MRAM and NATURE.
3. Design nano-wire and NASIC circuits.
4. Analyze CNT and design FPCNA.
5. Design the circuit using graphene transistor, RTD and QCA.

UNIT I	**FINFETS CIRCUIT DESIGN** Introduction of FinFETs – Shorted-Gate and Independent-Gate FinFETs – Logic Design using FinFETs – Threshold Voltage Control through Multiple Supply Voltages – The Principle of TCMS – Logic Design using TCMS – Schmitt Trigger using FinFETs – Latch Design using FinFETs – Precharge – Evaluate Logic Circuits using FinFETs – FinFET Layout – Oriented FinFETs.	**9**
UNIT II	**SRAM DESIGN AND HYBRID NANO CMOS SYSTEM** Fundamentals Nonplanar SRAM – Modeling of FinFET Devices for SRAM Applications – SRAM Design – Finfet Design for SRAM – NRAM – MRAM – PCM – Temporal Logic Folding – Architecture of Nature – Power Estimation – Nanomap Optimization Flow.	**9**
UNIT III	**CHARACTERIZATION TECHNIQUES, NANO WIRE ARRAYS AND NANOSCALE ASIC** Nanowires Fabrication Technologies – Crossbar Technologies – Architecture of Nanowire Crossbars - Testing Crossbars - NASIC Building Blocks – NASIC Circuit Styles – NASIC Logic Styles – NASIC Architectures.	**9**
UNIT IV	**CARBON NANOTUBE VLSI CIRCUITS AND FPCNA** CNTFET – Mis Positioned-CNT – Immune Logic Design – Design-Metallic CNT Immune CNFET Circuits – VLSI Compatible Metallic – CNT Removal – Design Flow – Nanoelectronic Devices – FPCNA Architecture – Nanotube LUT Fabrication.	**9**
UNIT V	**GRAPHENE TRANSISTOR, RTD AND QUANTUM CELLULAR AUTOMATE** Fabrication – Graphene Tansistors – Analog Circuits – Digital Circuits – Resonant Tunneling Diodes Fundamentals – QCA Fundamentals – Logic Design With QCA.	**9**
		Total: 45

REFERENCE BOOKS

1. Deming Chen and Niraj K. Jha., "*Nanoelectronic Circuit Design"*, Springer, 2011.
2. Nladimir V. Mitin,Viatcheslav A. Kochelap & Michael A. Stroscio., "*Introduction to Nanoelectronics Science, Nanotechnology, Engineering and Applications"*, Cambridge University Press.
3. Peter J.F. Harris, "*Carbon Nanotube Science Synthesis, Properties and Applications"*, Cambridge University Press.
4. Sze S.M., "*VLSI Technology"*, Mc.Graw.Hill Second Edition, 1998.
5. Goser K., Glosekotter P. Dienstuhl J., "*Nanoelectronics and Nanosystems from Transistors to molecular and quantum Devices"*, Springer, 2008.

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME III Semester under Regulations 2015
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit
Theory						
1	P15VLD509	**Professional Elective**- ASIC Design	3	0	0	3
2	P15VLD511	**Professional Elective**- Analysis and Design of Digital Integrated Circuits	3	0	0	3
3	P15VLD607	**Open Elective**- Human Resource Development	3	0	0	3
Practical						
4	P15VLD301	Project Phase - I	0	0	16	8
					Total Credits	**17**

Approved by

Chairman, Electronics and Communication Engineering BOS
Dr.R.S.Sabeenian

Member Secretary, Academic Council
Dr.R.Shivakumar

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

Copy to:-
HOD/ECE, Third Semester ME VLSI Students and Staff, COE

P15VLD509	ASIC DESIGN	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Explain the types of ASICs and design the CMOS logic cells.
2. Apply the concepts of programmable ASICs, programmable ASIC logic cells and programmable ASIC I/O cells.
3. Analyze and design the programmable ASIC interconnect and low level design language.
4. Write the code using Verilog and VHDL Logic synthesis and analyze the simulation process.
5. Illustrate and analyze the steps involved in floor planning, placement and routing.

UNIT I **INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN** **9**

Types of ASICs – Design Flow – CMOS Transistors CMOS Design Rules – Combinational Logic Cell – Sequential Logic Cell – Data Path Logic Cell – Transistors As Resistors - Transistor Parasitic Capacitance – Logical Effort – Library Cell Design - Library Architecture.

UNIT II **PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS** **9**

Anti Fuse – Static RAM – EPROM and EEPROM Technology – PREP Benchmarks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC – AC Inputs And Outputs – Clock & Power Inputs – Xilinx I/O Blocks.

UNIT III **PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY** **9**

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – Altera FLEX – Design Systems –Logic Synthesis – Half gate ASIC -Schematic Entry – Low Level Design Language – PLA Tools –EDIF –CFI Design Representation.

UNIT IV **ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING** **9**

System Partition – FPGA Partitioning – Partitioning Methods – Floor Planning – Placement – Physical Design Flow – Global Routing - Detailed Routing – Special Routing – Circuit Extraction – DRC.

UNIT V **ARCHITECTURE DESIGN AND CHIP DESIGN** **9**

Hardware Description Languages – Register- Transfer Design – High-Level Synthesis Architectures For Low Power – System-On-Chips and Embedded CPU's – Architecture Testing – Design Methodologies-Kitchen Timer Chip – Microprocessor Datapath.

Total: 45

REFERENCE BOOKS

1. Smith M.J.S, "Application *Specific Integrated Circuits",* Addison -Wesley Longman Inc, 2003.
2. Wayne Wolf., "*Modern VLSI Design System-On –Chip Design"*, Pearson Education, 2005.
3. Farzad Nekoogar and Faranak Nekoogar, "From *ASICs to SOCs: A Practical Approach"*, Prentice Hall PTR, 2003.
4. Wayne Wolf, "*FPGA-Based System Design"*, Prentice Hall PTR, 2004.

P15VLD511	ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

At the end of each unit, the students will be able to -

1. Explain the digital integrated circuits, devices-bipolar and MOS.
2. Analyze the fabrication, layout and simulation and MOS inverter circuits.
3. Analyze of the high speed CMOS logic design and dynamic logic design.
4. Discuss about the semiconductor memory design.
5. Examine the interconnect design and power grids.

UNIT I **DEEP SUBMICRON DIGITAL IC DESIGN, TRANSISTORS AND DEVICES** **9**

MOS AND BIPOLAR

Review of Digital Logic Gate Design-Digital IC Design – Computer Aided Design of Digital Circuits – The MOS Transistor – Bipolar Transistor And Circuits – IC Fabrication Technology – Layout Basics – Modeling The MOS Transistor for Circuit Simulation – SPICE MOS Level1 Device Model – BSIM3 Model-Additional Effects in MOS Transistors – SOI Technology.

UNIT II **FABRICATION, LAYOUT AND SIMULATION, MOS INVERTER CIRCUITS** **9**

Voltage Transfer Characteristics – Noise Margin Definitions – Resistive Load Inverter Design – NMOS Transistors as Load Devices – CMOS Inverter-Pseudo – NMOS Inverters – Sizing Inverters – Tristate Inverters.

UNIT III **HIGH SPEED CMOS LOGIC DESIGN, TRANSFER GATE AND DYNAMIC LOGIC DESIGN** **9**

Switching Time Analysis – Detailed Load Capacitance Calculation – Improving Delay Calculation With Input Slope - Gate Sizing For Optimal Path Delay – Optimizing Path With Logical Effort – Basic Concepts of Transfer Gate – CMOS Transmission Gate Logic – Dynamic D Latches And D Flip-Flops – Domino Logic – Voltage Bootstrapping.

UNIT IV **SEMICONDUCTOR MEMORY DESIGN, ADDITIONAL TOPICS IN MEMORY DESIGN** **9**

Introduction MOS Decoders – Static RAM Cell Design – SRAM Column I/O Circuitry – Memory Architecture – Content Addressable Memories – FPGA – Dynamic Read – Write Memories – Read Only Memories – EPROMs And EEPROMs – Flash Memory – FRAMs.

UNIT V **INTERCONNECT AND POWER GRID AND CLOCK DESIGN** **9**

Interconnect RC Delays – Buffer Insertion for Very Long Wires – Interconnect Coupling Capacitance – Interconnect Inductance – Antenna Effects – Power Distribution Design – Clocking and Timing Issues – Phase-Locked Loops – Delay-Locked Loops.

Total: 45

REFERENCE BOOKS

1. David A Hodges, Horace G Jackson, Resve A Saleh, "*Analysis and design of Digital Integrated Circuits – in deep submicron technology"*, Tata McGraw Hill, Edition 2005.
2. Sung-Mo Kang, Yusuf Leblebici, "*CMOS Digital Integrated Circuits-analysis and design"*, Tata McGraw Hill, Third edition, 2003.

SEMESTER - III

P15VLD607	**HUMAN RESOURCE DEVELOPMENT**	L:T:P:C	3:0:0:3

Course Outcomes : The Student will be able to:

1. Study the overview of Human Resource Development.
2. Understand the designing of HRD systems and developing HRD Strategies.
3. Study the methods of training and development for the employees.
4. Design performance appraisal system for managers.
5. Link HRD with the strategic plan of the organization

Unit	Syllabus Contents	Number of Sessions
1	**INTRODUCTION TO HRD** Nature and concept of HRD – Improving performance through HRD- Recent scenario of HRD in India- HRM and HRD – Role and Competencies of HRD manager- Challenges of HRD	9
2	**DESIGNING HRD SYSTEMS AND DEVELOPING HRD STRATEGIES** Subsystems of HRD - Designing HRD Strategy- HRD Strategy model- Future challenges to HRD Strategy.	9
3	**TRAINING AND DEVELOPMENT** Learning Cycle-Learning Process- objectives of training –Training need analysis- Training methods- Evaluation of Training - Designing management development Programs – Leadership development – Assessment and development center	9
4	**PERFORMANCE APPRAISAL AND POTENTIAL APPRAISAL** Designing Performance Appraisal System- Performance Appraisal Process- Methods of Performance Appraisal- Potential Appraisal-Matching Career Needs of Organization and Individual- Competency mapping - Career Planning Process- Employee Coaching – Process of Employee Counseling –Types of Mentoring	9
5	**QUALITY OF WORK LIFE AND STRATEGIC HRD** Empowering Employees- Need for Quality of work life- HRD Audit and Human Resource Accounting- HRD Culture – Linkage of Organizational Strategy to HRD Tactics- HRD and Organizational Change.	9
	Total No of Sessions	**45**

Learning Resources:

1	Text Books	1. Tapomoy Deb, Human Resource Development, Ane Books,2006 2. Mankin, D., *Human resource development,* Oxford University Press India,2015 3. Udai pareek., Designing & Managing Human resources sytems,2015
2	Reference Books	1. Haldar, U. K., *Human resource development,* Oxford University Press India,2015 2. Rao, T.V., Future of HRD, Macmillan Publishers India,2015 3. Nadler, L., Corporate human resources development, Van Nostrand Reinhold,2015 4. Cooper, Managing Stress, Sage, 2011
3	Web sites / links	1. http://forum.hrdiscussion.com/ 2. http://network.hrmtoday.com/forum 3. http://www.citeman.com/11853-evolution-of-the-concept-of-hrm/ 4. www.citehr.com 5. www.shrm.org

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME IV Semester under Regulations 2015
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit
Practical						
1	P15VLD401	Project Phase – II	0	0	24	12
					Total Credits	**12**

Approved by

Chairman, Electronics and Communication Engineering BOS
Dr.R.S.Sabeenian

Member Secretary, Academic Council
Dr.R.Shivakumar

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

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HOD/ECE, Fourth Semester ME VLSI Students and Staff, COE